Our Docket No.: 51876P567
Express Mail No.: EV 339916578US

UTILITY APPLICATION FOR UNITED STATES PATENT

FOR

SEMICONDUCTOR DEVICE HAVING ON-CHIP REFERENCE VOLTAGE GENERATOR

Inventor(s):
Young-Jae Cho
Seung-Hoon Lee

Blakely, Sokoloff, Taylor & Zafman LLP
12400 Wilshire Boulevard, 7th Floor
Los Angeles, CA 90025
Telephone: (310) 207-3800

SEMICONDUCTOR DEVICE
HAVING ON-CHIP REFERENCE VOLTAGE GENERATOR

Field of Invention

The present invention relates to a semiconductor device; and, more particularly, to an analog to digital converter (A/D converter) having an on-chip reference voltage generator.

Description of Prior Art

With the recent advance of CMOS VLSI technologies and digital signal processing techniques, high-definition video systems, next-generation personal mobile communication equipments, high-speed wireless networks, and medical imaging systems increasingly need high-resolution high-speed low-power A/D converters (hereinafter, referred to ADCs). Particularly, the ADCs for flat-panel displays, digital data storage read channels, medical imaging, and RGB graphic applications require at least 8-bit resolution and 200 MS/s performance with small chip area and low power consumption. Most of the conventional ADCs with a sampling rate exceeding 200 MS/s have been commonly based on flash, folding, subranging, and pipeline architectures. In this work, the pipeline architecture is employed to optimize speed, power consumption, and chip area.

Fig. 1 is a block diagram showing a conventional ADC.

As shown, the conventional ADC includes a sample and hold amplifier (hereinafter, referred to SHA) 11, first and second multiplying digital to analog converters 13 and 15 (hereinafter, referred to MDACs), first to third unit analog to digital converters 12, 14 and 16 (hereinafter, referred to UADCs), a digital correction logic 17 (hereinafter, referred to DCL) and a decimator 18 (hereinafter, referred to DCM).

In detail, the SHA 11 receiving an analog signal AIN is used for sampling of the inputted analog signal. The first to third UADCs 12, 14 and 16 respectively convert a sampling signal into a first-step digital code. Each of the first and second MDACs 13 and 15 converts each of the first-step digital codes outputted from the first to second UADCs into each of returned analog signals; subscribes the sampling signal by the returned analog signal; and, then, outputs a resultant signal to the second or third UADC 12, 14 and 16. After the sampling signal is converted into the first-step digital codes by the first to third UADCs 12, 14 and 16, the DCL 17 combines the first-step digital codes and outputs an 8-bit second-step digital code to the DCM. Lastly, the DCM 18 serves as sampling the 8-bit second-step digital code by 1/2 or 1/4 sampling rate. In addition, though there is not shown in Fig. 1, the conventional ADC uses an external clock signal or generates an internal clock signal in order to controlling the internal blocks described above.

Hereinafter, the operational step of the conventional ADC is described in detail.

First of all, the analog signal AIN is inputted to the conventional ADC and is sampled into the sampling signal by the SHA 11. Then, the first UADC 12 compares the sampling signal outputted from the SHA 11 with a reference voltage inputted from an external circuit and generates a first 3-bit first-step digital code.

Next, the first MDAC 13 converts the first 3-bit first-step digital code outputted from the first UADC 12 into a first returned analog signal. Then, the sampling signal is subscribed by the first returned analog signal. As a result, the first MDAC 13 can get a minute analog signal. The minute analog signal is amplified and outputted to the second UADC 14 and the second MDAC 15.

Then, like the first UADC 12, the second UADC 14 generates a second 3-bit first-step digital code. The second MDAC 15 is also operated like the first MDAC 13, and the third UADC 16 converts an outputted signal of the second MDAC 15 into a third 4-bit first-step digital code.

Next, the DCL 17 receives the first to third first-step digital codes outputted from the first to third UADC 12, 14 and 16. For removing nonlinearity errors, e.g., an offset voltage generated at an analog to digital conversion process, the DCL 17 superposes each of the last bit of the first 3-bit first-step digital code and the first bit of the second 3-bit first-step digital code upon each of the last bit of the second 3-bit first-step digital code and the first bit of the third 4-bit first-step digital code.

The conventional ADC uses the reference voltage in the operational step of converting an analog signal into a digital code or the digital code into the analog signal. In the conventional ADC, the reference voltage is supplied from an external circuit. If a reference voltage generator is in the external circuit, there is a filter between the reference voltage generator and the conventional ADC chip in order to stabilizing the reference voltage, i.e., removing a noise and a glitch generated by parasitic inductance and capacitance of a wire boning and an impedance of the conventional ADC chip.

In addition, for removing the noise and the glitch, capacitance of a capacitor included in the filter should be relatively large. As a result, because a size of the capacitor is enlarged in proportion to its capacitance, it is impossible that the reference voltage generator and the conventional ADC are encased in one chip.

Summary of Invention

It is, therefore, an object of the present invention to provide a semiconductor device which stabilizes a reference voltage by eliminating high frequency noise and glitch and has the advantages of a size and an operating speed.

In accordance with an aspect of the present invention, there is provided an analog to digital converter implemented in one chip including an on-chip reference voltage generator for generating N number of reference voltages, N being a

positive integer; and a conversion means for converting the inputted analog signal into a digital signal by using the reference voltages.

In accordance with another aspect of the present invention, there is provided a system having one chip analog to digital converter including an on-chip reference voltage generator contained in the analog to digital converter for generating N number of reference voltages, N being a positive integer; and a conversion block contained in the analog to digital converter for converting the inputted analog signal into a digital signal by using the reference voltages.

Brief Description of Drawings

The above and other objects and features of the present invention will become apparent from the following description of preferred embodiments taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing a conventional analog to digital converter (ADC);

Fig. 2 is a block diagram showing an ADC in accordance with the present invention;

Fig. 3 is a schematic circuit diagram describing an on-chip reference voltage generator and an RC filter shown in Fig. 2;

Fig. 4 is a capacitor included in the RC filter shown in Fig. 3;

Fig. 5 is a waveform demonstrating a simulation result of the on-chip reference voltage generator and the RC filter shown in Fig. 2;

Fig. 6 is a chip of the ADC in accordance with an embodiment of the present invention;

Fig. 7 is a waveform showing a differential nonlinearity DNL and an integral nonlinearity INL of the chip shown in Fig. 6;

Fig. 8 is a spectrum describing a digital code outputted from the chip shown in Fig. 6;

Figs. 9A and 9B are waveforms depicting each spurious free dynamic range SFDR and signal to noise and distortion ratio SNDR of the chip, shown in Fig. 6, per a sampling frequency and a frequency of an inputted signal; and

Fig. 10 is a graph showing a performance of the ADC in accordance with the present invention as compared with other ADCs.

Detailed Description of the Invention

Hereinafter, an analog to digital converter (A/D converter) having an on-chip reference voltage generator according to the present invention will be described in detail referring to the accompanying drawings.

Fig. 2 is a block diagram showing an analog to digital converter (hereinafter, referred to ADC) in accordance with the present invention.

As shown, the ADC is provided with an on-chip reference voltage generator 200 for supplying a reference voltage REF_VOL, an on-chip RC filter 300 for stabilizing the reference voltage REF_VOL and a conversion unit 100 for converting an analog signal AIN into an 8-bit digital signal DOUT.

The conversion unit 100 has the same structure with the conventional ADC shown in Fig. 1. Namely, the conversion unit 100 includes a sample and hold amplifier (hereinafter, referred to SHA) 110, first and second multiplying digital to analog converters 130 and 150 (hereinafter, referred to MDACs), first to third unit analog to digital converters 120, 140 and 160 (hereinafter, referred to UADCs), a digital correction logic 170 (hereinafter, referred to DCL) and a decimator 180 (hereinafter, referred to DCM). Thus, there is omitted a detailed description of structure and its operational steps.

However, for supplying the stable reference voltage, the ADC of the present invention impounds the on-chip reference voltage generator 200 and the conversion unit 100 in one chip. Moreover, the on-chip RC filter 300 is included in the same chip. As a result, because the reference voltage REF_VOL is generated inside the chip, integrity of the reference voltage REF_VOL is dramatically advanced. In attachment, unlike the prior art, the ADC of the present invention can be fabricated by a flip-chip packaging method as well as not a wire-bonding packaging method. Thus, integrity of the analog signal inputted to the SHA 110 is advanced.

Fig. 3 is a schematic circuit diagram describing the on-chip reference voltage generator 200 and the on-chip RC filter 300 shown in Fig. 2.

As shown, the on-chip reference voltage generator 200 includes an initial voltage generator 220 for generating an initial voltage VREFIN, a voltage level shifter 240 for generating reference voltages REFT and REFC by shifting a level of the initial voltage VREFIN and a voltage driver 260 for outputting the stabilized reference voltages REFTOP and REFBOT to the conversion unit 100 by stabilizing the reference voltages REFT and REFC.

The on-chip RC filter 300 coupled between the on-chip reference voltage generator 200 and the conversion unit 100 includes two pair of a resistor and a capacitor serially connected to each other.

In detail, the voltage level shifter 240 includes a first voltage inducing block 242 for receiving the initial voltage VREFIN and inducing an induced voltage TR2, a first driving block PM1 for supplying an operating current and a voltage dividing block 244 for outputting the reference voltages REFT and REFC based on the induced voltage TR2 and the operating current. The voltage level shifter 240 further includes a first capacitor C1 coupled between the voltage inducing block 242 and the voltage dividing block 244 for stabilizing the reference voltages REFT and REFC.

In addition, the voltage driver 260 includes a first driving unit for outputting the first stabilized reference

voltage REFTOP by stabilizing the first reference voltage REFT and a second driving unit for outputting the second stabilized reference voltage REFBOT by stabilizing the second reference voltage REFC.

The on-chip reference voltage generator 200 includes the operational steps of generating the initial voltage VREFIN; generating the first and second reference voltages REFT and REFC by adjusting level of an induced voltage in response to the initial voltage VREFIN; and outputting the first and second stabilized reference voltages REFTOP and REFBOT by stabilizing the first and second reference voltages REFT and REFC.

Fig. 4 is a filtering capacitor included in the on-chip RC filter 300 shown in Fig. 3.

As shown, the filtering capacitor is implemented by a PMOS transistor. Gate G of the PMOS transistor is one side of the filtering capacitor, and source S, drain D and body B as the other side of the filtering capacitor are coupled to the supply voltage VDD. Herein, for decreasing a body effect of the PMOS transistor, the source S and the drain D of the filtering capacitor are connected to the body B of the filtering capacitor. In compared with a general capacitor having a metal-insulator-metal (MIM) structure, the filtering capacitor of the present invention using the PMOS transistor can have a larger capacitance versus its size.

Fig. 5 is a graph demonstrating a simulation result of the on-chip reference voltage generator 200 and the on-chip RC

filter 300 shown in Fig. 2.

As shown, time is the value of a coordinate on an x-axis of the graph (unit is ns) and the reference voltage is the value of a coordinate on a y-axis of the graph (unit is mV). In the graph, there are a solid line and a dotted line: the solid line is the reference voltage of the present invention; and the dotted line is the reference voltage of the prior art.

Two different circuits operating at the speed of 220 MS/s are simulated and compared. The conventional ADC has 0.1 uF off-chip bypass capacitors at reference voltage output nodes and the ADC of the present invention has the on-chip RC filter 300 connected to the reference voltage output nodes. As illustrated in Fig. 4, a settling time of the circuit with the on-chip RC filter 300 is 0.45 ns which can be corresponding to the higher sampling rate than 400 MS/s. However, the settling time with the 0.1 uF off-chip capacitors at the reference outputs get clearly much longer. Bonding pads based on this specific package are assumed to have the parasitic inductance and capacitance of 2.5 nH and 0.7 pF, respectively. Herein, the settling time is defined as a time needed for stabilizing the reference voltage in the range of $\pm 2mV$.

Fig. 6 is a chip of an ADC in accordance with an embodiment of the present invention.

The ADC in accordance with an embodiment of the present invention is fabricated in a 0.25 um n-well single-poly, five-metal CMOS process. The die photograph of the ADC is shown in

Fig. 6. The on-chip PMOS decoupling capacitors between circuit blocks are indicated by the bold dotted lines.

The ADC in accordance with the embodiment of the present invention employs a MCS technique in the 3b MDACs for having low power consumption and low noise at high speed. The MCS technique reduces the required MDAC unit capacitors from 8 to 4 by merging two unit capacitors into a single capacitor based on the equal charge redistribution concept. When using the same unit capacitor size as a conventional MDAC, the SHA and the MDAC improve the amplifying speed without increasing power consumption by reducing the load capacitances of the SHA and the number of the interconnection lines and the required devices in the MDAC by 50%. The unit capacitor sizes in the first and the second 3b MDACs are 100fF and 50fF, respectively, considering power consumption, resolution, kT/C noise, and 8b matching. The MDACs are based on a two-stage amplifier constituting with a folded-cascode and an unfolded-cascode architectures in the first and second stages, respectively, with the DC gain of 70 dB. The -3 dB frequencies of the first and second MDACs are 562 MHz and 477 MHz, respectively. The ADC occupies the active die area of 2.25 mm^2 and dissipates 220 mW at 2.5 V and 220 MS/s.

Fig. 7 is a waveform showing a differential nonlinearity DNL and an integral nonlinearity INL of the chip shown in Fig. 6. As illustrated, the measured DNL and INL are within -0.44 to +0.43 LSB and -1.13 to +0.83 LSB.

Fig. 8 is a spectrum describing a digital code outputted

from the chip shown in Fig. 6.

As shown, the spectrum measured with a 120 MHz analog sine wave at 220 MS/s is plotted. The output digital data are captured at the quarter rate (1/4) of the 220 MHz clock with the on-chip decimator circuits. It is noted that the ADC itself is operating at the full speed of 220 MS/s.

Figs. 9A and 9B are graphs depicting each spurious free dynamic range SFDR and signal to noise and distortion ratio SNDR of the chip, shown in Fig. 6, per a frequency of a sampling frequency and an inputted signal.

When the sampling rate is increased from 50 MS/s to 220 MS/s, the SNDR and the spurious-free dynamic range (SFDR) with a 10 MHz differential input sine wave are shown in Fig. 9A. The SNDR is maintained above 40 dB when the sampling frequency increases up to 200 MS/s. The SNDR decreases from 41 dB to 38 dB by 3 dB with a 10 MHz input at the maximum operation sampling rate of 220 MS/s. The actual dynamic performance of the ADC at the maximum operating frequency is expected to be better, considering the parasitic capacitance and inductance components in bonding wire lines whose horizontal and vertical lengths are 1.1 mm and 1.2 mm in this current packaged version, respectively. Since the proposed ADC will be integrated as one of several important core macro cells for a relatively big system and will have short input and output interconnection lines, such long bonding wire problems as observed in this multi-project wafer (MPW) based package will rarely happen.

The SNDR and the SFDR in Fig. 9B are measured with increasing input frequencies at the maximum sampling frequency of 220 MS/s. With the input frequencies increased to a Nyquist frequency, the SNDR and the SFDR are maintained over 37 dB and 49 dB, respectively. The measured performance of the ADC in accordance with the present invention is summarized in Table 1.

Resolution		**8 bits**
Max. Rate		**220 MS/s**
Process		**0.25 um CMOS**
Input Range		**1 V_{p-p}**
SNDR	**at 200 MS/s**	**40.8 dB at 10 MHz, 40.1 dB at 120 MHz, 37.4 dB at 500 MHz**
	at 220 MS/s	**38.0 dB at 10 MHz, 36.9 dB at 120 MHz, 34.3 dB at 500 MHz**
SFDR	**at 200 MS/s**	**49.5 dB at 10 MHz, 49.3 dB at 120 MHz, 47.2 dB at 500 MHz**
	at 220 MS/s	**47.3 dB at 10 MHz, 48.6 dB at 120 MHz, 41.4 dB at 500 MHz**
DNL		**-0.44 LSB / +0.43 LSB**
INL		**-1.13 LSB / +0.83 LSB**
ADC Core Power		**220 mW at 220 MS/s**
Active Die Area		**2.25 mm^2 (= 1.5 mm × 1.5 mm)**

Table 1. Performance summary of the ADC in accordance with the present invention

Fig. 10 is a graph showing the performance of the ADC in accordance with the present invention as compared with other ADCs.

As shown, an ADC using a bipolar transistor consumes large power and an ADC using a CMOS transistor of the prior

art can not be fabricated with one chip. However, the ADC in accordance with the present invention can impound all of component in the one chip and have advantages of an operating speed, a size and power consumption. Herein, the figure of merit (FoM) which is the value of a coordinate on a y-axis of the graph is defined as a following equation.

$$FOM = (2 \times ERBW) \times 2^{ENOB} / POWER \quad \text{(unit: MHz/mW)} \quad \text{Eq. 1}$$

In the Eq. 1, the effective resolution bandwidth (ERBW) is the input frequency where the signal-to-noise ratio (SNR) decreases by 3 dB below the SNR at low input frequencies and the ENOB represents the effective number of bits of the ADCs.

Consequently, the analog to digital converter (ADC) having the on-chip reference voltage generator and the on-chip RC filter can effectively remove a noise or a glitch by impounding the on-chip reference voltage generator and the on-chip RC filter in a chip of the analog to digital converter.

As described above, the on-chip reference voltage generator and the on-chip RC filter in accordance with the present invention are applied to the ADC. However, the present invention can be employed to a semiconductor device using a reference voltage, e.g., a digital to analog converter DAC, a filter and so on.

While the present invention has been described with respect to the particular embodiments, it will be apparent to those skilled in the art that various changes and modification may be made without departing from the spirit and scope of the invention as defined in the following claims.